

General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

Application

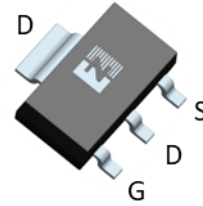
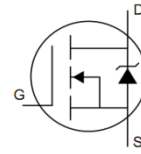
- SMPS 2nd Synchronous Rectifier
- BLDC Motor driver

Product Summary

$$V_{DS} = 60V$$

$$R_{DS(ON)} = 50m\Omega$$

$$I_D = 9A$$



SOT-223

Ordering Information:

Part NO.	ZM500N06E
Marking	500N06
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

Absolute Maximum Ratings ($T_c = 25^\circ C$)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_{D@TC=25^\circ C}$	9.0	A
	$I_{D@TC=75^\circ C}$	6.8	A
	$I_{D@TC=100^\circ C}$	5.6	A
Pulsed Drain Current ^①	I_{DM}	27	A
Total Power Dissipation	$P_D@T_c=25^\circ C$	8	W
Total Power Dissipation ^②	$P_D@T_A=25^\circ C$	1	W
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Storage Temperature	T_{STG}	-55 to 150	$^\circ C$
Single Pulse Avalanche Energy@L=0.1mH	E_{AS}	10	mJ
ESD Level (HBM)		CLASS 1B	

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case ^②	R_{thJC}	-	-	15	° C/W
Thermal resistance, junction - ambient	R_{thJA}	-	-	120	° C/W
Soldering temperature, wavesoldering for 10s	T_{sold}	-	-	265	° C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2		2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=8A$		50	65	m Ω
		$V_{GS}=4.5V, I_D=6A$		62	85	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=5A$		4		s
Source-drain voltage	V_{SD}	$I_S=8A$			1.28	V

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Gate Resistance	R_g	$f = 1MHz$		1.9		Ω
Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V$ $f = 1MHz$	-	823	-	pF
Output capacitance	C_{oss}		-	33	-	
Reverse transfer capacitance	C_{rss}		-	19	-	

•Gate Charge characteristics($T_a = 25^\circ C$)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q_g	$V_{DD}=25V$ $I_D=8A$ $V_{GS}=10V$	-	11	-	nC
Gate - Source charge	Q_{gs}		-	2.5	-	
Gate - Drain charge	Q_{gd}		-	1.5	-	

Fig.1 Gate-Charge Characteristics

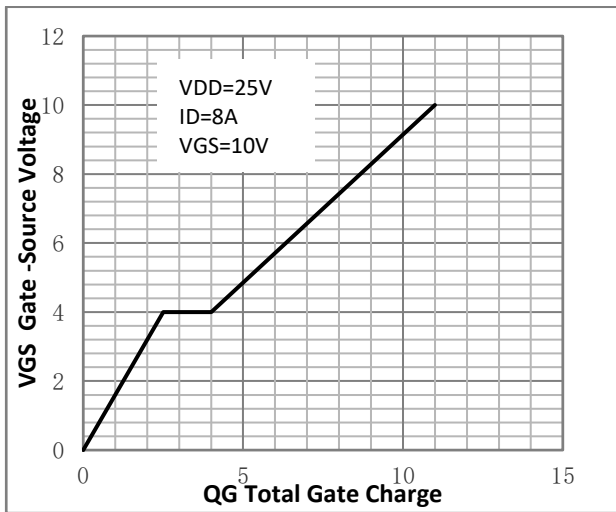


Fig.2 Capacitance Characteristics

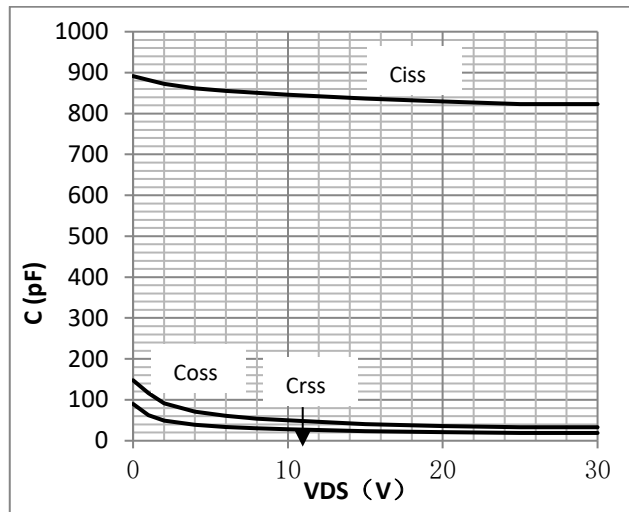


Fig.3 Power Dissipation Derating Curve

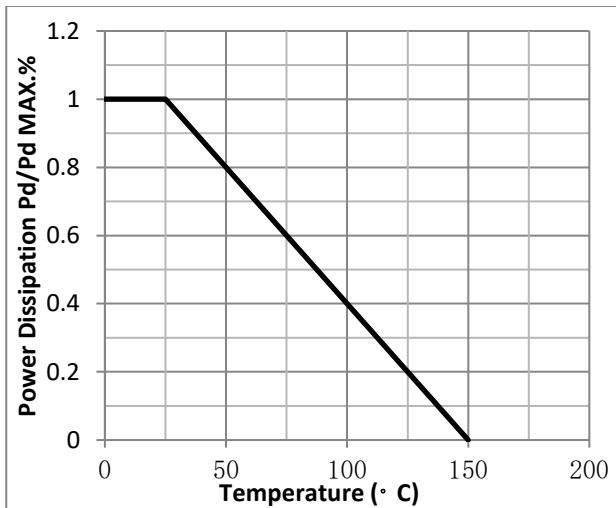


Fig.2 Typical output Characteristics

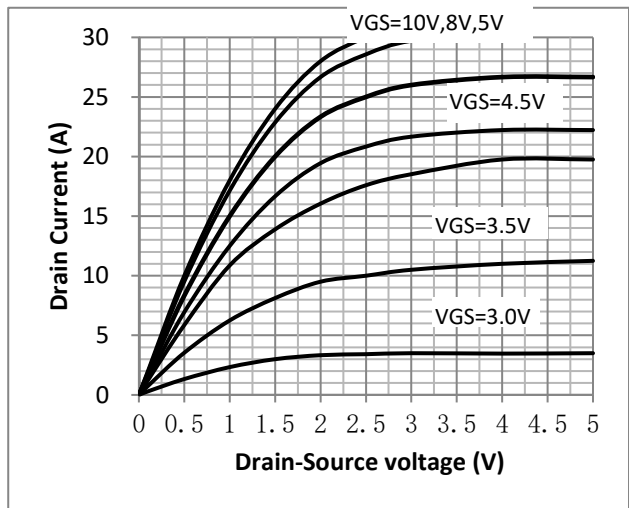


Fig.3 Threshold Voltage V.S Junction Temperature

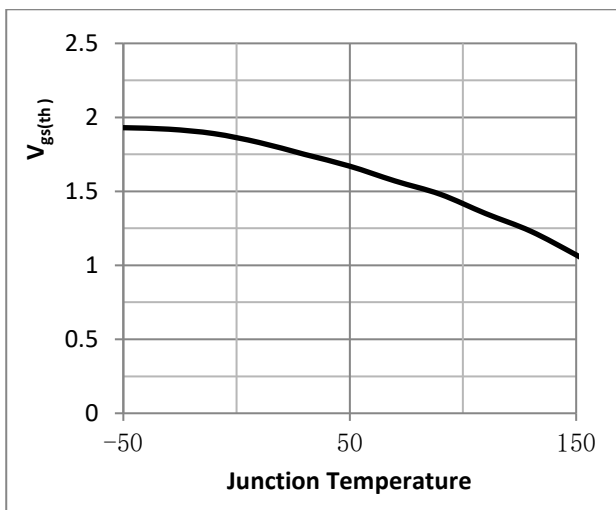


Fig.4 Resistance V.S Drain Current

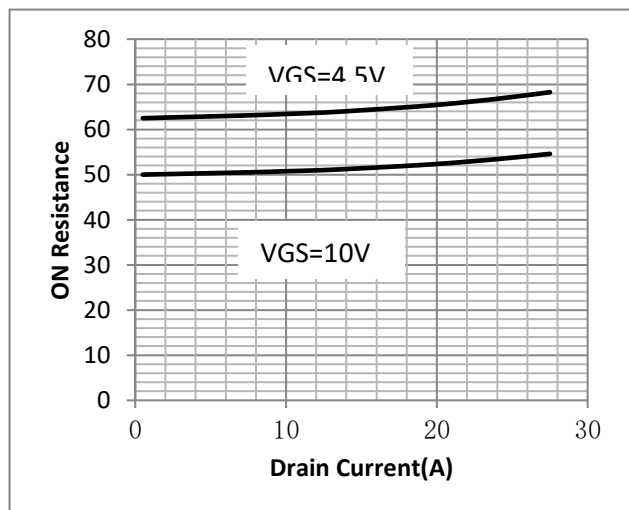


Fig.5 On-Resistance VS Gate Source Voltage

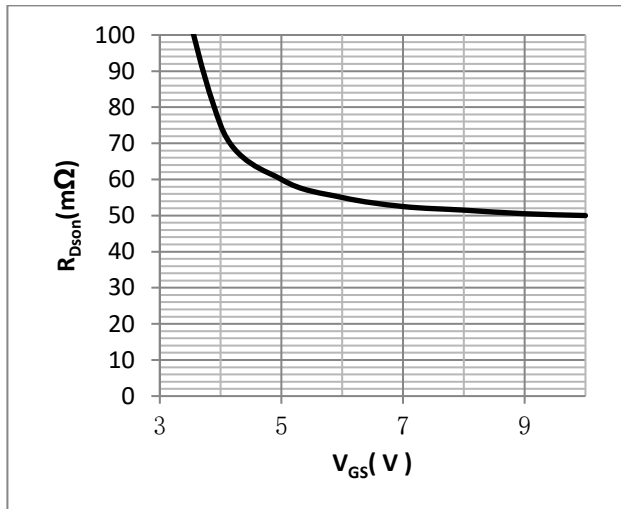


Fig.6 On-Resistance V.S Junction Temperature

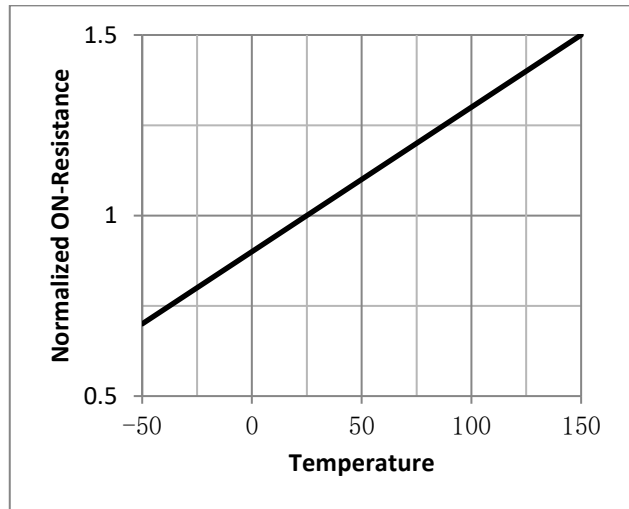


Fig.9 SOA Maximum Safe Operating Area

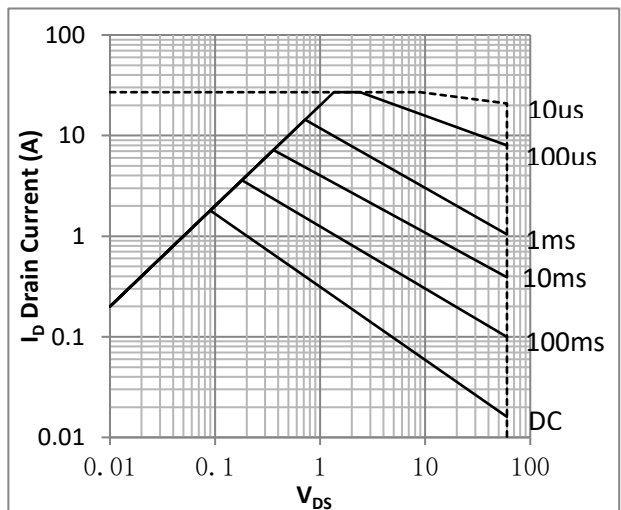


Fig.10 I_D -Junction Temperature

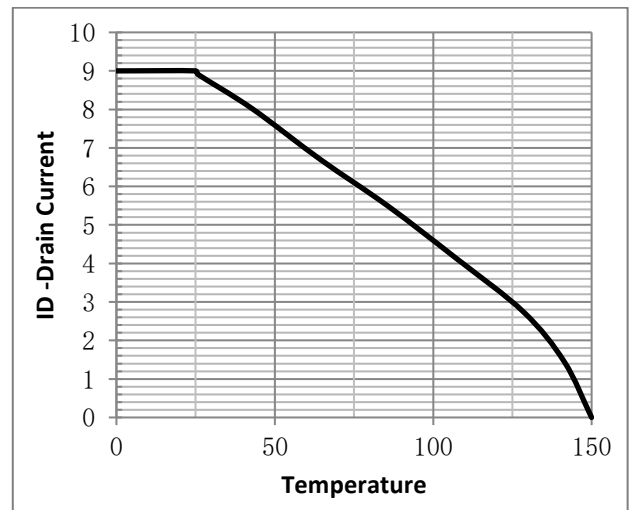


Figure 11. Diode Forward Voltage vs. Current

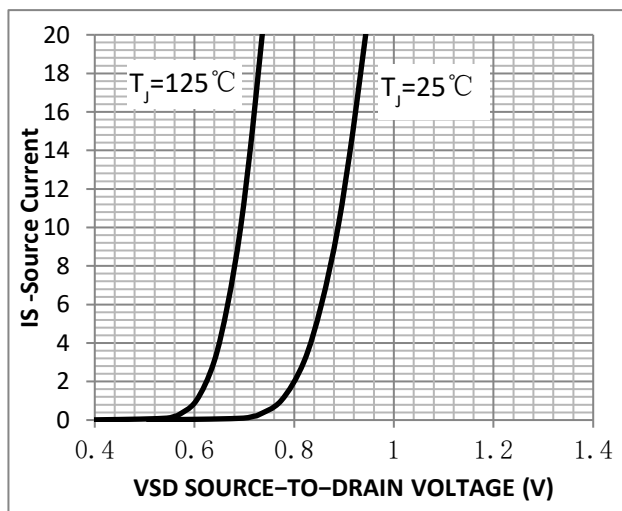


Figure 12. Transfer Characteristics

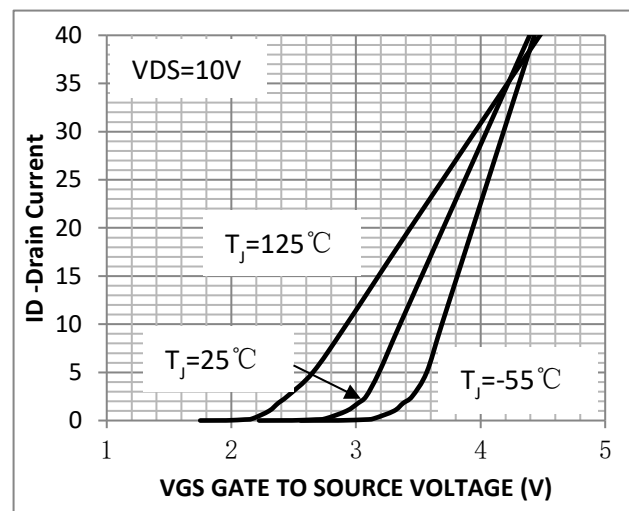


Fig.7 Gate Charge Measurement Circuit

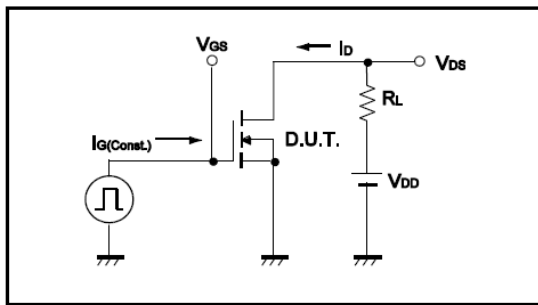


Fig.8 Gate Charge Waveform

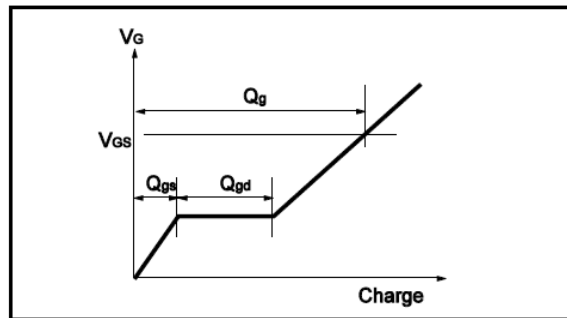


Fig.9 Switching Time Measurement Circuit

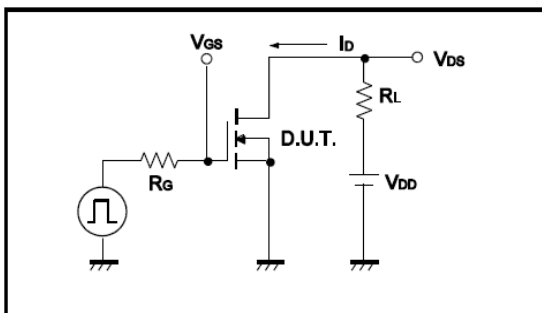


Fig.10 Switching Time Waveform

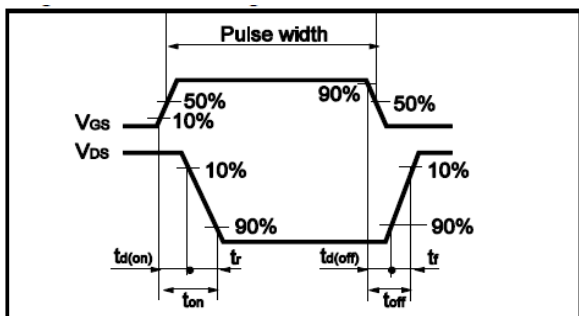


Fig.11 Avalanche Measurement Circuit

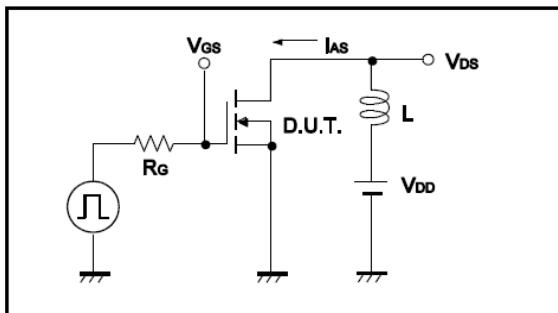
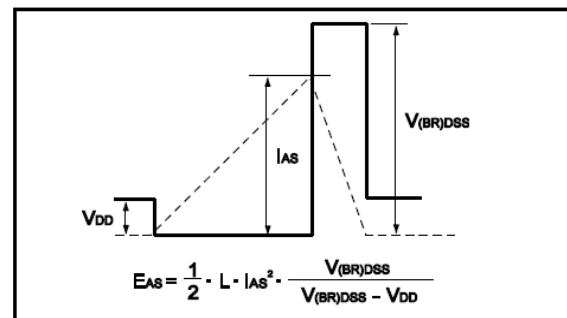
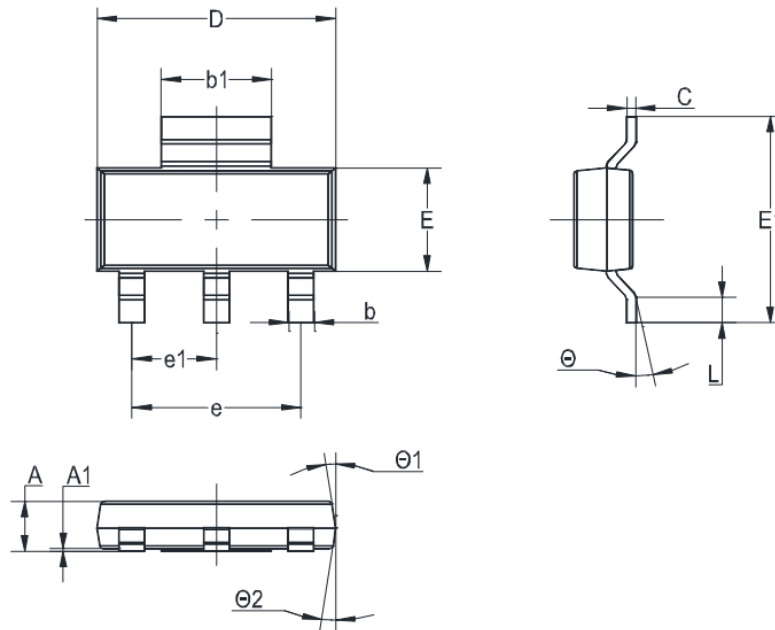


Fig.12 Avalanche Waveform

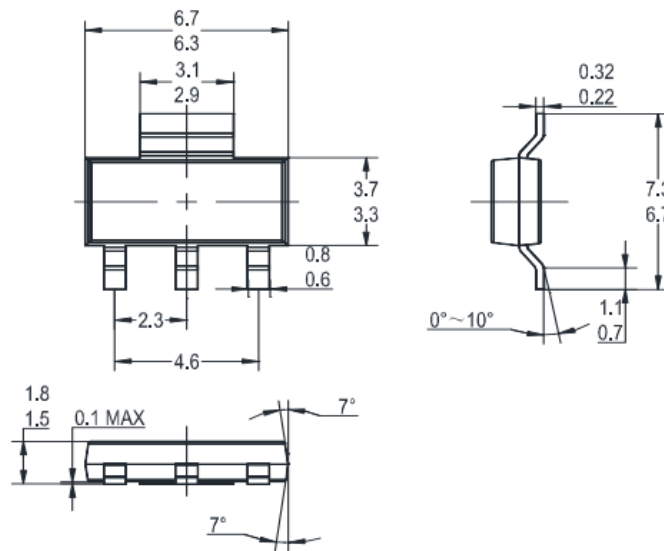


•Dimensions(SOT-223)

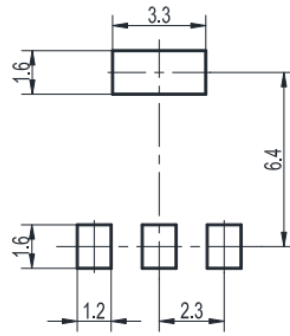
Unit: mm



Unit	A	A1	b	b1	C	D	E	E1	e	e1	L	Θ	$\Theta1$	$\Theta2$
mm	1.8 1.5	0.1 MAX	0.8 0.6	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	7.3 6.7	4.6 TYP	2.3 TYP	1.1 0.7	10° 0°	7° 0°	7° 0°



Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
SOT-223	12	8 ± 0.1	0.315 ± 0.004	330	13	3,000

Note: ① Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$;

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;

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